Faculty Profile

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1. Name of Faculty: Dr.Hemant Motilal Pardeshi
2. Present Position : Lecturer Electronics
3. Address : 1301, Vijeta B, Dosti Vihar, Vartak Nagar, Thane,
4. 400606
5. Mobile No. : 8169479348
6. E-Mail Id : pardeshi.ju@gmail.com
7. Date of joining (Govt of Maharashtra) : 3/04/2001

(Govt. Poly. Mumbai) : 2/8/2014

1. Total Teaching Experience in years: 20 Years 9 month
2. Memberships of professional organizations/Bodies : Life Member ISTE

**QUALIFICATIONS: (Graduation and Onwards)**

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| **Sr.**  **No.** | **Degree** | **University** | **Class Award** | **Year of Passing** |
| 01 | PhD | Jadavpur University, Kolkata |  | 2014 |
| 02 | M.E (Electronics) | Dr. BAMU, Aurangabad | Distinction | 2005 |
| 03 | B.E (E & TC) | SRTMU, Nanaded | Distinction | 1999 |

**CAREER DETAILS:**

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| **Sr. No.** | **Organization** | **Designation** | **Duration** | **Period** | **Work Done in Brief** |
| 01 | Government Polytechnic, Mumbai | Lecturer | 20 Years | 2001-till date | Student Mentoring, Lab development, Student Counseling. |

**TRAINING COURSES ATTENDED:**

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| **Sr. No.** | **Course Name** | **Duration** | **Place** | **Training Agency** | **Remarks** |
| 1 | Induction Training Phase-I | 2 Weeks | Aurangabad | DTE, Mumbai |  |
| 2 | Induction Training Phase-II | 2 Weeks | Bhopal | NITTR,Bhopal |  |
| 3 | Industrial Training | 8 Weeks | Aurangabad | Government Polytechnic Aurangabad |  |

**Publications:**

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| 1 | Hemant Pardeshi, “Analog/RF Performance of AlInN/GaN Underlap DG MOS-HEMT”, *Superlattices and Microstructures*, Vol. , (2015). Published by Elsevier. Impact Factor : 2.1 |
| 2 | Hemant Pardeshi, C K Sarkar, et.al., “Investigation of Asymmetric Effects Due to Gate Misalignment, Gate Bias and Underlap Length in III-V Heterostructure Underlap DG MOSFET”, *Physica-E*, Vol. 46, (2012)*.* Published by Elsevier. Impact Factor : 2.0 |
| 3 | Hemant Pardeshi, C K Sarkar, et.al., “Influence of barrier thickness on AlInN/GaN underlap DG MOSFET device performance”, *Superlattices and Microstructures*, Vol. 60, (2013). Published by Elsevier. Impact Factor : 2.1 |
| 4 | Hemant Pardeshi, C K Sarkar, et.al., “Performance assessment of gate material engineered AlInN/GaN underlap DG MOSFET for enhanced carrier transport efficiency”, *Superlattices and Microstructures*, Vol. 60, (2013). Published by Elsevier. Impact Factor : 2.1 |
| 5 | Hemant Pardeshi, C K Sarkar, et.al., “Effect of Underlap and Gate length on device performance of AlInN/GaN Underlap MOSFET”, *Journal of Semiconductors*, Vol. 33, No 12, (2012). Published by IOP Science. |
| 6 | Hemant Pardeshi, C K Sarkar, et.al., “Comparative Assessment of III-V Heterostructure and Silicon Underlap Double Gate MOSFETs”, *Semiconductors*, Vol. 46, No. 10, (2012). Published by Springer. Impact Factor : 1.6 |
| 7 | Hemant Pardeshi, C K Sarkar, et.al., “Polarization based charge density drain current and small-signal model for nano-scale AlInGaN/AlN/GaN HEMT devices”, *Superlattices and Microstructures*, Vol. 54, (2013). Published by Elsevier. Impact Factor : 2.1 |
| 8 | Hemant Pardeshi, C K Sarkar, et.al., “Impact of gate length and barrier thickness on performance of InP/InGaAs based Double Gate Metal Oxide Semiconductor Heterostructure Field-Effect Transistor (DG MOS-HFET)”, *Superlattices and Microstructures*, Vol. 55, (2013). Published by Elsevier. Impact Factor : 2.1 |
| 9 | Hemant Pardeshi, C K Sarkar, et.al., “Flicker and thermal noise in an n-channel Underlap DG FinFET in a weak inversion region”, *Journal of Semiconductors*, Vol. 34, No. 02, (2013). Published by IOP Science. |
| 10 | Hemant Pardeshi, C K Sarkar, et.al., “Analysis of Ficker and Thermal noise in p-channel Underlap DG FinFET”, *Microelectronics Reliability*, Vol. 54, (2014). Published by Elsevier. Impact Factor : 1.6 |
| 11 | Hemant Pardeshi, C K Sarkar, et.al., “Study of HfAlO/AlGaN/GaN MOS-HEMT with source field plate structure for improved breakdown voltage”, *Physica E*, Vol 46, ( 2015). Published by Elsevier. Impact Factor : 2.0 |
| 12 | Hemant Pardeshi, C K Sarkar, et.al., “High performance AlInN/AlN/GaN p-GaN Back Barrier Gate-Recessed Enhancement-Mode HEMT”, *Superlattices and Microstructures*, Vol. 75, (2015). Published by Elsevier. Impact Factor : 2.1 |
| 13 | Hemant Pardeshi, C K Sarkar, et.al., “Physics based charge and drain current model for AlGaN/GAN HEMT devices”, *Journal of Electron Devices*, Vol. 14, 2012. |
| 14 | Hemant Pardeshi, C K Sarkar, et.al., “Performance Analysis of AlInN/GaN Underlap DG MOSFET for varying Underlap and Gate length”, *IJCA* Issue 4, 2013. ISSN for IJCA Digital Library is 0975 - 8887. |
| 15 | Hemant Pardeshi, C K Sarkar, et.al., “Analytical Drain Current Model for Symmetrical Gate Underlap DG MOSFET”, *IJCA* Issue 4, 2013. ISSN for IJCA Digital Library is 0975 - 8887. |
| 16 | Hemant Pardeshi, C K Sarkar, et.al., “Comparison study of Drain Current, Subthreshold Swing and DIBL of III-V Heterostructure and Silicon Double Gate MOSFET”, *IJECT*, Vol. 4, Issue Spl - 1, 2013. ISSN: 2230-7109 (Online). |
| 17 | Hemant Pardeshi, C K Sarkar, et.al., “Comparative Assessment of Ground Plane and Strained Based FDSOI MOSFET”, *Informacije MIDEM,* Vol. 75, (2015). Impact Factor: 0.6. |
| 18 | Hemant Pardeshi, et.al., “Comparison Assessment of InGaAs/In Pans Silicon based DG MOS-HEMT”, *IJARSE*, Vol. 4, Issue Spl - 1, 2015. ISSN: 2319-8354 (Online). |
| 17 | Hemant Pardeshi, C K Sarkar, et.al., (2015), “Effect of AIN Spacer layer thickness on Device performance of AlInN/AIN/GaN MOSFET”, *International Conference onComputing Communication Control and Automation (ICCUBEA-*2015*,Feb* 26-27, 2015. Pune, India. (IEEE explore) Awarded Best Paper |
| 18 | Hemant Pardeshi, et.al., (2015), “Effect of gate length variation on DC Performance of In0.7Ga0.3As/InAs/In0.7Ga0.3As Composite Chanel HEMT”, *International Conference on Computer Graphics, Vision and Information Security (CGVIS -2015) , Nov* 2-3, 2015. KIIT University, Bhubaneshwar, India. (IEEE explore) |
| 19 | Hemant Pardeshi, C K Sarkar, et.al., (2012), “Effect of Barrier layer thickness on device performance of AlInN/GaN Underlap DG MOSFET”, *International Conference on Communications, Devices and Intelligent Systems (CODIS-2012) December*  28-29, 2012. Jadavpur University, Kolkata, India. (IEEE explore). |
| 20 | Hemant Pardeshi, C K Sarkar, et.al., (2012), “Performance Analysis of AlInN/GaN Underlap DG MOSFET for varying Underlap and Gate length”, *International Conference on Communication, Circuits & Systems (iC3S-2012), October* 5-7, 2012. KIIT University, Bhubaneshwar, India. |
| 22 | Hemant Pardeshi, C K Sarkar, et.al., (2012), “Analytical Drain Current Model for Symmetrical Gate Underlap DGMOSFET”, *International Conference on Communication, Circuits & Systems (iC3S-2012),October*  5-7, 2012. KIIT University, Bhubaneshwar, India. |
| 23 | Hemant Pardeshi, C K Sarkar, et.al., (2011), “Influence of Underlap length on Short Channel Effects in 18nm Gate Length Double Gate MOSFET”, *International Workshop on Future of Nano Electronics Research & Challenges Ahead, December*  25-27, 2011. SKP College of Engg. Tirunammalai, India. |
| 24 | Hemant Pardeshi, C K Sarkar, et.al., (2011), “DC and Breakdown voltage analysis of 27 nm gate length AlGaAs/InGaAs HEMT”, *International Workshop on Future of Nano Electronics Research & Challenges Ahead, December*  25-27, 2011. SKP College of Engg. Tirunammalai, India. |
| 25 | Hemant Pardeshi, C K Sarkar, et.al., (2012), “Performance Comparison of III-V Heterostructure and Silicon Double Gate MOSFET”, *2nd International Conference on Advances in Engineering and Technology ( ICAET 2012), December*  20-22, 2012. EGS Pillay COE, India. Published by : CIIT. |

**Specialization/ Area of Interest:**

1. Simulation of Heterostructure Devices MOSFETs.
2. Compound Semiconductor Devices.
3. GaN Based Advanced MOS Devices.

**Portfolios handled at institute level (Last 3 years):**

1. DTE/ RO Mumbai – Inspection / Enquiry Committee members /Admission
2. MSBTE / RBTE – Inspection / Enquiry Committee members
3. MSBTE/ RBTE - Inspection / Enquiry Committee members
4. Paper Setter/Moderator for MSBTE/Govt. Aided/ Aided instiutes
5. BOS member K J Somaiya Polytechnic
6. External Examiner for OR/PR/Project at other institutes
7. DSR Verification/ Store Verification
8. Officer Incharge Proof reading, Audit – GPM Exam
9. Reviewer for International Technical Journal of Global Importance
10. MHRD-PWD Scheme Departmental Coordinator
11. State Level Covid awareness Quiz

**Portfolios handled at department level (Last 3 years):**

1. NBA coordinator
2. CEP/STTP/Testing/Consultancy Co-Ordinator
3. Implant Training Co-Ordinator
4. Incubation Co-Ordinator EC Dept
5. Project Mentoring for project Competition
6. Lab Incharge 310
7. Extra Lecture conduction (Direct 2nd year Students)
8. Organized Expert Lectures for 3rd Year Students
9. Project Guide